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EXAMINER	
LOUIE, OSCAR A	

ART UNIT	PAPER NUMBER
2136	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mN

Office Action Summary	Application No.	Applicant(s)	
	10/814,691	O'CONNOR, DENNIS M.	
	Examiner	Art Unit	
	Oscar A. Louie	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8-10,20,23,24 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 4, 6, 8-10, 20, 23, 24, & 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This final action is in response to the amendment filed on 08/02/2007. The examiner acknowledges the applicant's amendments to the drawings and claims. In light of the applicant's amendments, the examiner hereby withdraws his 35 U.S.C. 112 1st paragraph rejection of Claim 15. Claims 1, 3, 4, 6, 8-10, 20, 23, 24, & 26-29 are pending and have been considered as follows.

Claim Objections

1. Claims 9, 26, & 28 are objected to because of the following informalities:

- Claim 9 line 1 contains the term "capable" which the examiner recommends changing to "configured to."
- Claim 26 line 2 contains the term "capable" which the examiner recommends changing to "configured to."
- Claim 28 line 2 contains the term "operable" which the examiner recommends changing to "configured to."

Appropriate correction is required.

Allowable Subject Matter

2. Claims 3, 4, 26, & 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6, 8-10, 20, 23, 27, & 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sibert (US-7124170-B1) in view of Mahon et al. (US-4809160-A).

Claim 1:

Sibert discloses a processor comprising,

- "a mechanism to identify memory as secure memory accessible by secure processes, and to identify non-secure memory accessible by both secure and non-secure processes" (i.e. "FIG. 3 shows software running on SPU 100 that includes both protection-critical software 202 and other software 201") [column 6 lines 53-55];
- "a security enforcement mechanism to allow page tables for the non-secure processes to be stored in secure memory" (i.e. "That is, external bus 104 provides output-only addressing, but can transfer data for both input and output purposes") [column 6 lines 48-53];

but does not disclose,

- "a translation look-aside buffer (TLB)"
- "wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process"

however, Mahon et al. do disclose,

- "The Target Register 70 as shown in FIG. 3 contains the return address in Address Location 300 with the original, lower privilege level stored in two lower order bits 310. The TLB 30 then checks the access rights of the calling instruction as will be described shortly to determine if execute access is permitted" [column 3 lines 41-46]

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a translation look-aside buffer (TLB)" and "wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process," in the invention as disclosed by Sibert since a translation look-aside buffer would be commonly used to check the access rights of instructions particularly when dealing with memory access.

[Where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly Applicant claims a combination that only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d at 1518-19 (BPAI, 2007) (citing KSR, 127 S.Ct. at 1740, 82 USPQ2d at1396. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.]

Claim 6:

Sibert and Mahon et al. disclose a processor, as in Claim 1 above, further comprising,

- "virtual address translation hardware to perform virtual address translation for non-secure processes via page tables in secure memory" (i.e. "Such dual decoding permits SPU monitor 203 to use a single address mapping (mapping some logical address to the physical page or pages where all control registers are present compactly) for system control purposes") [column 14 lines 46-49].

Claim 8:

Sibert and Mahon et al. disclose a processor, as in Claim 1 above, further comprising,

- "a control register to specify whether page tables for non-secure processes are kept in secure memory or nonsecure memory" (i.e. "In such embodiments, processor security registers 132 can be used to indicate which internal resources permit or do not permit such external access") [column 6 lines 53-55].

Claim 9:

Sibert and Mahon et al. disclose a processor, as in Claim 1 above, further comprising,

- "page table walk hardware capable of accessing secure memory on behalf of non-secure processes" (i.e. "In other embodiments, external bus 104 may also be designed to support input addressing, so that external devices (including other processors) can initiate "direct memory access" (DMA) to the internal resources, memory, and/or other components of SPU 100") [column 6 lines 48-53].

Claim 10:

Sibert discloses a processor comprising,

- "an apparatus to differentiate between hardware generated memory accesses and software generated memory accesses" (i.e. "memory management unit 131, which is used by monitor 203 to isolate memory regions accessible to different software modules. Memory management unit 131 can employ a variety of familiar mechanisms to effect such isolation, including paging, page protection, segmentation, segment limits, protection domains, capabilities, storage keys, and/or other techniques") [column 7 lines 55-62];
- "to grant secure memory access to hardware generated memory accesses" (i.e. "the translation tables are kept in internal memory 102 in order to guarantee their integrity and to ensure that only monitor 203, and specific authorized hardware functions (e.g., the MMU) can manipulate them") [column 8 lines 1-4];

but does not disclose,

- "wherein the hardware generated memory accesses are the result of a translation lookaside buffer (TLB) miss that occurs when the processor is running in a non-secure mode"
- "wherein the secure memory access occurs without the processor leaving the non-secure mode"

however, Mahon et al. do disclose,

- "The Target Register 70 as shown in FIG. 3 contains the return address in Address Location 300 with the original, lower privilege level stored in two lower order bits 310.

The TLB 30 then checks the access rights of the calling instruction as will be described shortly to determine if execute access is permitted" [column 3 lines 41-46];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "wherein the hardware generated memory accesses are the result of a translation lookaside buffer (TLB) miss that occurs when the processor is running in a non-secure mode" and "wherein the secure memory access occurs without the processor leaving the non-secure mode," in the invention as disclosed by Sibert since a translation look-aside buffer miss indicates that no virtual address is mapped to a physical address, which would be implied since hardware generated memory accesses would have direct memory access.

[Where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly Applicant claims a combination that only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d at 1518-19 (BPAI, 2007) (citing KSR, 127 S.Ct. at 1740, 82 USPQ2d at1396. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.]

Claim 20:

Sibert discloses a method comprising,

- "determining if a current process page table is in secure or non-secure memory in a non-secure process running in a processor's non-secure mode" (i.e. "FIG. 3 shows software running on SPU 100 that includes both protection-critical software 202 and other software 201") [column 6 lines 53-55];
- "if the current process page table is in non-secure memory, performing the page table walk in non-secure memory" (i.e. "a "non-critical only" attribute for the page table it designates, the attribute indicating that the page base addresses in level-two page table 305 can designate only "non-critical" memory regions") [column 11 lines 30-33];

but does not disclose,

- "determining if a translation look-aside buffer (TLB) miss has occurred in a non-secure process running in a processor's non-secure mode"
- "if the current process page table is in secure memory, performing a page table walk in secure memory without leaving the non-secure mode"

however, Mahon et al. do disclose,

- "The Target Register 70 as shown in FIG. 3 contains the return address in Address Location 300 with the original, lower privilege level stored in two lower order bits 310. The TLB 30 then checks the access rights of the calling instruction as will be described shortly to determine if execute access is permitted" [column 3 lines 41-46];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "determining if a translation look-aside buffer (TLB) miss has occurred in a non-secure process running in a processor's non-secure mode" and "if the current process page table is in secure memory, performing a page table walk in secure memory without leaving the non-secure mode," in the invention as disclosed by Sibert since a translation look-aside buffer would be commonly used to check the access rights of instructions particularly when dealing with memory access.

[Where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly Applicant claims a combination that only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d at 1518-19 (BPAI, 2007) (citing KSR, 127 S.Ct. at 1740, 82 USPQ2d at1396. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.]

Claim 27:

Sibert discloses a processor comprising,

- "secure memory accessible when the processor is in a privileged secure mode or a user secure mode" (i.e. "Certain regions of physical memory (most importantly, some or all of internal memory 102) can be designated "critical" and access to those regions restricted to certain processor operating modes") [column 8 lines 47-50];

- "non-secure memory accessible when the processor is in a privileged non-secure mode or a user non-secure mode" (i.e. "A "non-critical only" protection attribute can be used to designate certain translation tables as being permitted to specify address translations only to "non-critical" addresses") [column 8 lines 51-54];

but does not disclose,

- "a security enforcement mechanism that allows access to page tables in secure memory when a translation look-aside buffer (TLB) miss occurs in the user non-secure mode"
- "wherein the access to the page table occurs without the processor leaving the user non-secure mode"

however, Mahon et al. do disclose,

- "The Target Register 70 as shown in FIG. 3 contains the return address in Address Location 300 with the original, lower privilege level stored in two lower order bits 310. The TLB 30 then checks the access rights of the calling instruction as will be described shortly to determine if execute access is permitted" [column 3 lines 41-46]

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a translation look-aside buffer (TLB)" and "wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process," in the invention as disclosed by Sibert since a translation look-aside buffer would be commonly used to check the access rights of instructions particularly when dealing with memory access.

[Where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727,

1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly Applicant claims a combination that only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d at 1518-19 (BPAI, 2007) (citing KSR, 127 S.Ct. at 1740, 82 USPQ2d at1396. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.]

Claim 29:

Sibert and Mahon et al. disclose a processor, as in Claim 27 above, further comprising,

- "a memory management unit to access the page table while the processor remains in the user non-secure mode" (i.e. "Both software 201 and software 202 may comprise many modules, only some of which may be resident in secure memory 102 at any particular time. Software modules will typically be resident in separate memory spaces and have access to memory spaces controlled by monitor 203 so that they are effectively isolated from each other") [column 7 lines 2-8].

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sibert (US-7124170-B1) in view of Mahon et al. (US-4809160-A) and in further view of Mel et al. ("Tablet: Personal Computer of the Year 2000").

Claim 24:

Sibert discloses an electronic system comprising,

- "memory that can be partitioned by the processor into secure memory accessible by secure processes and non-secure memory accessible by secure or nonsecure processes" (i.e. "Both software 201 and software 202 may comprise many modules, only some of which may be resident in secure memory 102 at any particular time. Software modules will typically be resident in separate memory spaces and have access to memory spaces controlled by monitor 203 so that they are effectively isolated from each other") [column 7 lines 2-8];
- "wherein the processor includes a security enforcement mechanism to allow page tables for non-secure processes to be stored in secure memory" (i.e. "Both software 201 and software 202 may comprise many modules, only some of which may be resident in secure memory 102 at any particular time. Software modules will typically be resident in separate memory spaces and have access to memory spaces controlled by monitor 203 so that they are effectively isolated from each other") [column 7 lines 2-8];

but does not disclose,

- "the processor includes a translation look-aside buffer (TLB)"

- "wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process"
- "a plurality of antennas"
- "an amplifier coupled to at least one of the plurality of antennas to amplify communications signals"
- "a processor coupled to the amplifier"

however, Mahon et al. do disclose,

- "The Target Register 70 as shown in FIG. 3 contains the return address in Address Location 300 with the original, lower privilege level stored in two lower order bits 310. The TLB 30 then checks the access rights of the calling instruction as will be described shortly to determine if execute access is permitted" [column 3 lines 41-46];

but the combination of Sibert and Mahon et al. do not disclose,

- "a plurality of antennas"
- "an amplifier coupled to at least one of the plurality of antennas to amplify communications signals"
- "a processor coupled to the amplifier"

whereas, Mel et al. do disclose,

- "The main use for the cellular link will be to communicate with other computers and the people using them" [page 642];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "the processor includes a translation look-aside buffer (TLB)" and "wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process" and "a plurality of antennas" and "an amplifier coupled to at least one of the plurality of antennas to amplify communications signals" and "a processor coupled to the amplifier," in the invention as disclosed by Sibert since a translation look-aside buffer would be commonly used to check the access rights of instructions particularly when dealing with memory access to control devices of a computing system such as a communications interface card with an antenna.

[Where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly Applicant claims a combination that only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d at 1518-19 (BPAI, 2007) (citing KSR, 127 S.Ct. at 1740, 82 USPQ2d at1396. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.]

Response to Arguments

6. Applicant's arguments filed 08/02/2007 have been fully considered but they are not persuasive.

- Applicant's arguments regarding independent Claims 1, 10, 20, 24, & 27 have been considered above in the standing 35 U.S.C. 103(a) rejections and are moot in view of the new ground(s) of rejection as necessitated by the applicant's amendments. The examiner notes that the KSR ruling based rejections above were necessitated by the applicant's amendments. The amendments included the limitations of some of the dependent claims, brought into their respective independent parent claim(s) that were already rejected as a combination under 35 U.S.C. 103(a) in the previous rejection.
- Regarding dependent Claims 3, 4, 26, & 28, the examiner hereby withdraws his previous rejections for Claims 3, 4, 26, & 28 in light of the applicant's amendments and arguments. Claims 3, 4, 26, & 28 are thereby objected to as allowable subject matter as stated above.

Conclusion

7. Applicant's arguments filed 08/02/2007 have been fully considered but are moot in view of the new ground(s) of rejection as necessitated by the applicant's amendments.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
10/12/2007

Nasser Moazzami
Supervisory Patent Examiner

10/15/07